AMENDMENTS TO THE SPECIFICATION

Amend the paragraph found on page 3, lines 12-17 as set forth below:

Another method used by real-time bus controllers ~~are~~ is to implement so-called "filter registers ~~registers~~." Filter registers ~~register~~ are complemented by hardware comparators ~~allowing~~ to bring some "relief" for the CPU(s) by reducing the interrupt rate and reducing time consuming message address compare operations. The message IDs to be filtered are stored in specific registers, e.g. 16 identifiers, and are compared with the message approaching on the bus. Only messages having matching identifiers are forwarded to the CPU.

Amend the paragraph found on page 8, lines 16-23 as set forth below:

Each of the four CAN-busses 202 to 205 is connected to one of the ~~a~~ respective bus adapters 214 to 217. The bus adapters 214 to 217 might be formed by standardized CAN controllers providing connections to the respective CAN-busses 202 to 205 via CAN-C or CAN-B physical layers. On one hand, each bus adapter 214 to 217 has ~~got~~ a connection to an interrupt request bus 220. On the other hand, each bus adapter 214 to 217 ~~possess~~ possesses a connection to a multiplexer 222. The connections to the multiplexer 222, however, might be formed by a bus providing ~~a~~ sets of conductors, such as wires, PCB (printed circuit board) tracks or connections to an integrated circuit, to connect the bus adapters 214 to 217 with the multiplexer 222.

Amend the paragraph found from page 8, line 24 through page 9, line 5 as set forth below:

Corresponding to the four bus adapters 214 to 217, both CPUs 207 and 208 are ~~as well~~ also connected to the interrupt bus 220 and to the multiplexer 222. The multiplexer 222 further shows a connection to a control engine 224 of ~~a~~ an IP (initializing process) execution unit 226 and to ~~an~~ a transmission unit 228, which is included in a PP (presentation process) execution unit 230. A controller 232 controls the multiplexer 222 in response to control signals transmitted over dedicated control signal lines received by the first CPU 207, the second CPU 208 and the transmission unit 228, respectively. The arrangement as drawn above enables the multiplexer to provide connections from the bus adapters 214 to 217 and the CPUs 207 and 208 to either ~~to~~ the control engine 224 or the transmission unit 228.

Amend the paragraph found from page 19, lines 20-26 as set forth below:

Further advantages of the intercommunication preprocessor according to the present invention are in particular that only a comparably ~~comparable~~ small amount of hardware gates are requirements, leading to low system cost. Furthermore, this reduces the system power consumption, as well as the physical size, and increases the reliability. The intercommunication preprocessor advantageously relieves the load on the master CPU by reducing the workload on the master CPU induced by bridge, router and gateway functions to a minimum. Thus, the CPU has more computation power for the system applications. The functionality of the overall system is increased by powerful message filtering.